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DESIGN AND ANALYSIS OF PHASE LOCKED LOOP

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Research Article

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Abstract

This study employs the 45nm CMOS technology (GPDK045library) in the CADENCE Vertuoso Analog Design Environment to develop a PLL system. The proposed PLL architecture comprises the following modules: a voltage controlled oscillator to produce the clock output, which is the multiplication of the input reference frequency and multiplication factor (N); a phase and frequency detector (PFD) to compare the phase (or frequency) of the input reference and the phase (or frequency) of the feedback signal and generate the difference or an error signal; a charge pump and loop filter to convert the digital UP and DOWN signals into analog control voltage; and a frequency divider to equalize the output frequency with the input frequency. With a lock time of 40µs, all modules are combined to generate a 1GHz output frequency from a 4MHz input frequency using a 1.8V DC supply. The output clock has a 44.87 ps period jitter.

Keywords: voltage controlled oscillator, phase locked loop, charge pump, phase and frequency detector, and lock time.

I. INTRODUCTION

A crucial component of contemporary electrical and communication systems is the phase-locked loop (PLL). The PLL is most often employed in microprocessor, communication, and networking systems for clock generation and recovery. In order to comprehend a larger lock range PLL with shorter lock time, a lot of study has recently been conducted on the PLL, and research is currently ongoing. Since advancements in integrated circuits, PLL has emerged as a key component of electronics technology. Because PLL architecture incorporates both digital and analog signal circuits, it functions similarly to a mixed signal circuit, posing high frequency design issues.

Phase and frequency detector (PFD), charge pump (CP), loop filter (LPF), voltage controlled oscillator, and frequency divider are the five primary components of a typical phase-locked loop. Analog PLL (APLL), Digital PLL (DPLL), and All Digital PLL (ADPLL) are the three kinds of PLL architectures now in use for PLL design. The PFD compares the feedback signal (VCO output) with the reference input signal in the proposed PLL block diagram (Fig. 1), producing two output signals—up and down pulses—that are dependent on the phase and frequency difference between the reference and feedback signals. In order to increase or decrease the VCO output frequency, UP and DOWN signals are applied to the charge pump, which transforms them into analog current that flows into or out of the loop filter that is charging or discharging the capacitor. The frequency divider then divides the VCO output frequency by 256, which equals the reference frequency. This process continues until the phase locks.

II. PRIOR WORK

The majority of electrical and communication systems in use today have various processor types that run on high frequency clocks. These processors often get their clocks from local oscillators, which are low frequency clocks with a typical frequency of 10 to 100 MHz. PLL, which just multiplies the low frequency reference clock by a multiplication

factor to get the high frequency clock, is required if we want high frequency clocks. Setting the delay of each stage in a digitally controlled oscillator is challenging, and DCOs have increasingly intricate designs. By using a second oscillator to provide the reference frequency, the conventional design uses more space to produce an 800 MHz output from a 100 MHz input. An architecture that uses the lowest input frequency and VCO rather than DCO to produce a 1GHz output from a 4MHz input is used to get around all of these issues.

III. Architecture and Circuit Design

The PLL is widely used in microcontrollers to regulate the frequency of clock signals. This can give the opportunity for microcontroller to run at frequency of the clock is faster than the oscillator itself. This research suggests an analog PLL design technique for charge pump-based PLLs. The design of a gigahertz phase-locked loop on 45nm CMOS technology is the primary goal of this research. Phase and frequency detector (PFD), charge pump (CP), loop filter (LPF), voltage controlled oscillator (VCO), and frequency divider (÷256) are the five modules that make up the suggested PLL design.

A. Frequency and Phase Detector

As shown in Fig. 2, it generates the error or difference signal by comparing the input reference signal and feedback signal. The phase difference ($\Delta\varnothing$) between its two inputs determines its output in a linear fashion.

Two D-flip flops and an AND gate make up the PFD's schematic construction, which is seen in Fig. 2. VDD is linked to the data terminal of the top D-flip flop, while the clock terminal receives the reference input signal (Fref). The data terminal of a bottom D-flip flop is linked to VDD, and the clock terminal receives a feedback signal (Ffbk). Both D-flip flops' reset terminals receive the reset signal. Initially, up = dn = 0. When Fref rises, the up signal rises as well. Eventually, the rising edge of Ffbk follows, and the dn signal rises as well. The NAND gate then resets both signals. As an alternative, state that up and dn signals represent temporary increases. However, the difference between their average values accurately depicts the input signals' frequency or phase discrepancy. As can be seen in Fig. 2, a buffer is positioned at each output side to power the subsequent step.

Fig 3 (a)and (b) shows the output waveforms of the PFD for two conditions i) phase of input reference signal (Fref) leads phase of feedback signal (Ffbk) and ii) phase of input reference signal (Fref) lags phase of feedback signal (Ffbk).

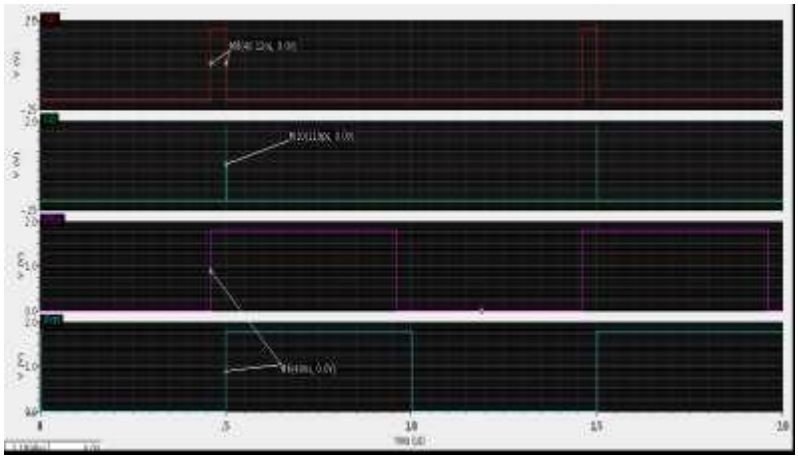


Fig.3(b): PFD output when reference signal(Fref) lags Ffbk.

A. Charge Pump and Loop Filter

Charge pump circuit is used to combine the both PFD outputs (UP and DOWN) and gives the single output IP, which is utilized to charge or discharge the capacitor in loop filter.

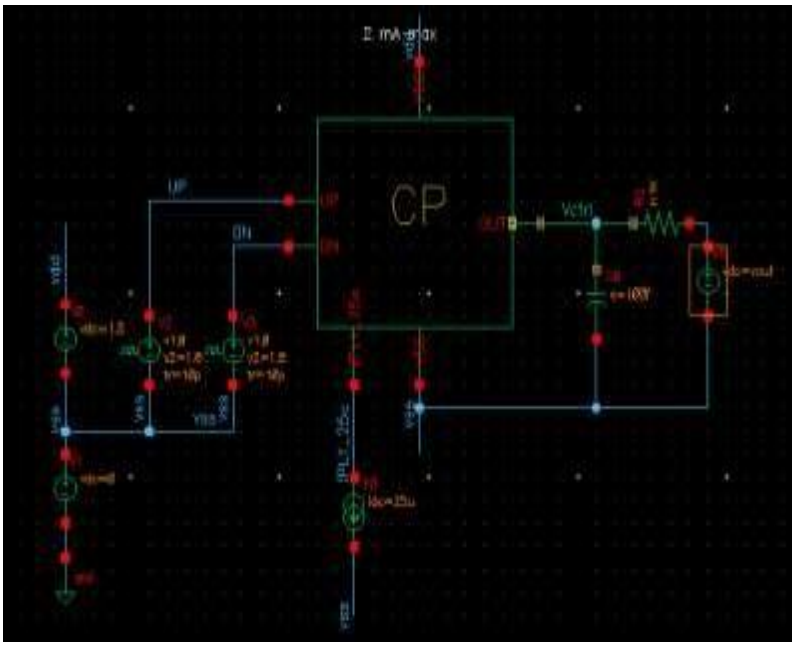


Fig.4: Charge pump circuit

Source current is enabled when the UP signal is high. This means that source current will enter the loop filter, charge the capacitor, raise the control voltage, and ultimately raise the VCO output frequency. As illustrated in Figure 5, when both UP and DOWN signals are low, no current will flow into the loop filter, resulting in constant voltage and constant VCO output. Conversely, when DOWN signal is high, sink current enables, i.e. sink current flows out of the loop filter, discharges the capacitor, and lowers the control voltage, which lowers the VCO output frequency.

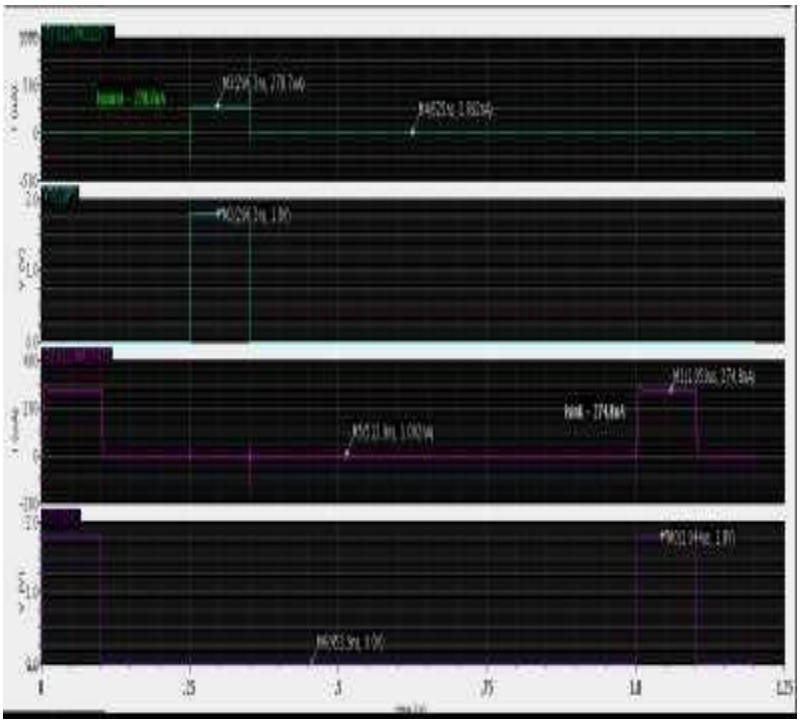


Fig.5: Charge pump output waveform.

B. Voltage Controlled Oscillator

Voltage Controlled Oscillator is most important block in PLL as shown in Fig.6. VCO generates clock signal and its output frequency can be varied by changing the input control voltage.

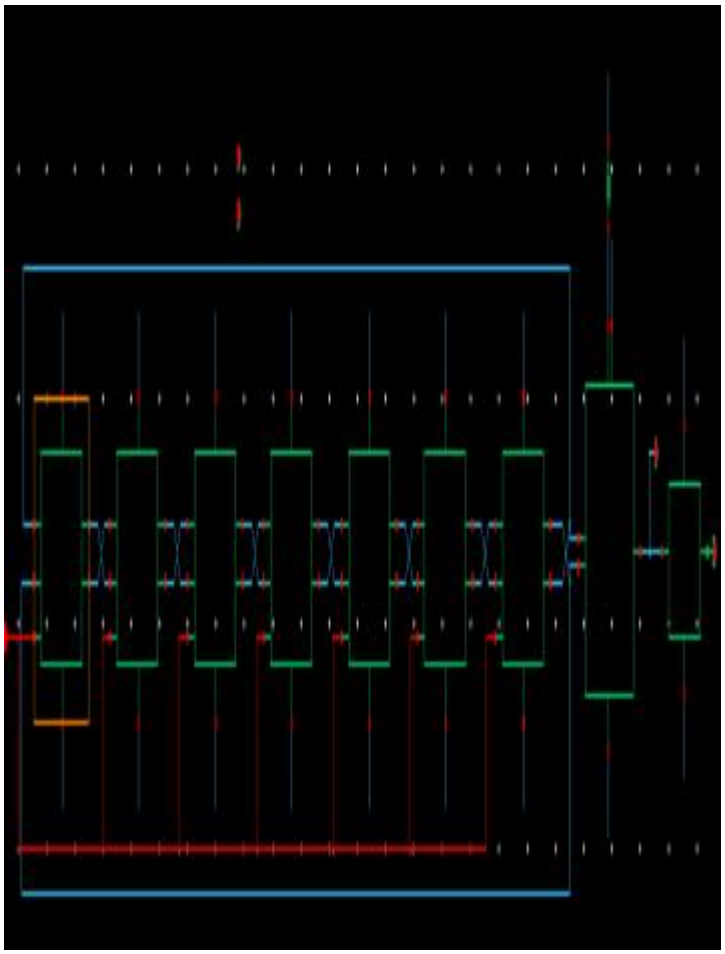


Fig.6: Voltage controlled oscillator circuit.

The most popular CMOS oscillator in modern technology is the ring oscillator. Single ended ring oscillators have trouble determining the time delay (Td) because to circuit parasites and nonlinearities. Here, I used a differential ring oscillator, which comprises seven gain stages in a loop with an inversion between each step, as seen in fig. 6, to prevent the oscillation speed and multiphase output from conflicting. In addition to producing a 50% duty cycle at the output, this circuit has improved immunity to common mode noise and is not limited to an odd number of stages, which allows for greater flexibility in adjusting the oscillation frequency due to the high frequency tuning range of ring oscillators. The frequency of oscillation is provided by

,

$$F_{out} = \frac{1}{2NT_d} \quad (1)$$

Where, N - Number of stages. Td - delay of each cell,

$$\therefore T_d = \frac{1}{2NF_{out}}$$

Given, Fout = 1GHz and N=7

$$\therefore T_d = \frac{1}{2x7x1x10^9} = 71.42ps$$

As shown in Fig. 7, the output frequency is 1.00 GHz at Vctrl=1.187. The output frequency changes in tandem with changes in the control voltage (Vctrl). The output frequency vs input control voltage (Vctrl) plot in Figure 8 illustrates the transfer characteristics of the vco. From this figure, we can determine the vco gain, or Δ = 0.705G, and conclude that the circuit should be linear. As seen in Fig. 8, the vco output frequency range is 110.4MHz to 1.88GHz for lowest control voltage Vctrl = 0.7V and 1.88GHz for maximum control voltage Vctrl = 1.8V.

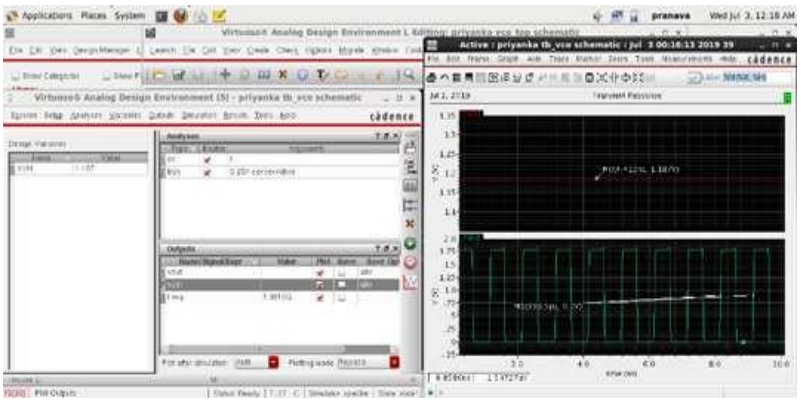


Fig.7: VCO output waveform.

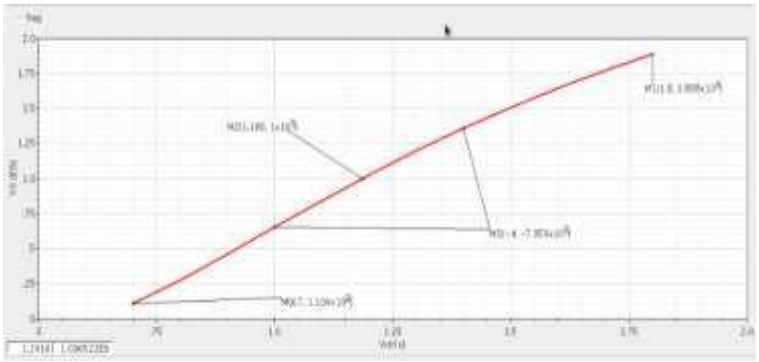


Fig.8: Transfer characteristics of VCO.

C. Frequency Divider

Function of the frequency divider is to scales down the VCO output frequency by a factor N and equals to input reference frequency. This circuit as shown in Fig.9 which is placed in between the VCO and PFD circuit, that is in feedback path.

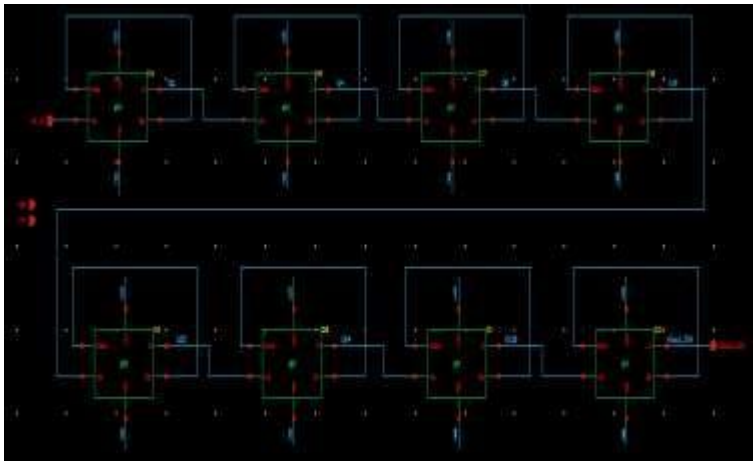


Fig.9: Frequency divider circuit(÷256).

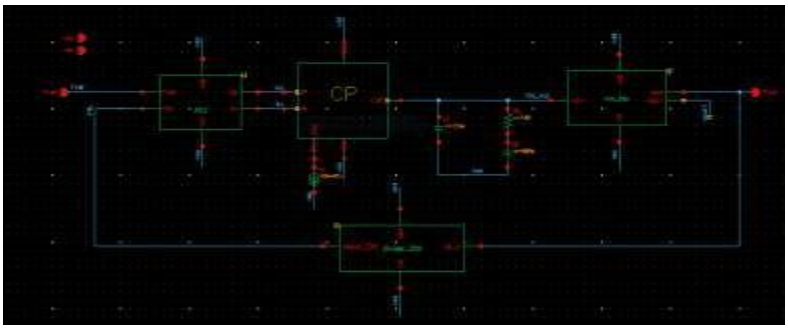


Fig.10: Proposed PLL Architecture.

All above explained circuits are integrated in order to generate the 1GHz output from 4MHz input as shown in Fig.10. The PLL is in locked condition at 1GHz and within 40µs time cycle.

IV. RESULT

We develop and simulate the integrated Phase Locked Loop circuit. Figure 12 illustrates the change in the control voltage. When the reference input signal (Fref) and feedback signal (Fout) are locked, the loop filter circuit's output indicates that the control voltage (Vctrl) stays constant. It is evident from Fig. 12 that the control voltage stays at a steady 0.885V for the whole 40µs time cycle.

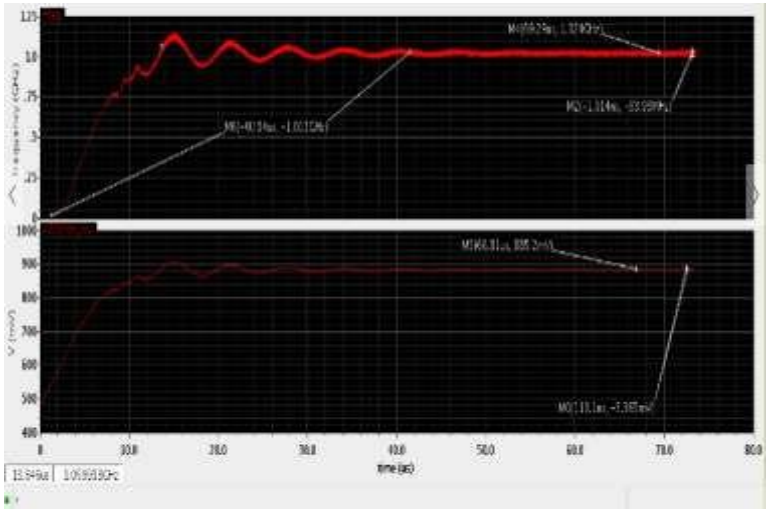


Fig.11. Output frequency and control voltage(Vctrl) versus time.

The PLL is locked at 1GHz frequency as shown in Fig.11. Time elapsed between PLL power on and the time at which 1GHz occur is called lock time. The lock time is 40µs. PLL output have jitter = 44.87ps as shown in Fig.11.

TABLE I: Performance summary and Comparison of traditional PLL with proposed PLL.

References	[1]	[3]	Conventional work.	Proposed work
Technology	180nm	130nm	90nm	45nm
Supply voltage	1.2V	1V	1V	1.8V
Frequency range	155.4MHz	100-400MHz	100MHz-1GHZ	4MHz

Locked time	X	X	2.82ns	40µs
period jitter	X	5.81ps	4.223ps	44.87ps

V. CONCLUSION

Redesigning the PLL using 45nm CMOS technology to generate a 1GHz output frequency from a 4MHz input reference frequency at a supply voltage of 1.8V is the primary goal of this project. Despite being in lock mode, the PLL output remains constant after completion of this process. The output frequency of this design is calculated by multiplying the input reference frequency (4MHz) by the integer factor (256). Additionally, the lock time (40µs) and period jitter (44.87ps) are determined. It is possible to utilize this PLL design as a frequency multiplier.

The suggested design is used for clock systems and other analog applications. to create a digitally controlled oscillator for various digital applications, as well as to further decrease the lock time and construct a programmable divider for several electronics and radio frequency applications. It may serve as a useful guide for future PLL design utilizing various methodologies.

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